

WE CLAIM:

1 1. An RF semiconductor device comprising:
2 a high resistivity polysilicon handle wafer;
3 a buried oxide layer over the polysilicon
4 handle wafer; and,
5 a silicon layer over the buried oxide layer.

1 2. The RF semiconductor device of claim 2
2 further comprising an RF input.

1 3. An RF semiconductor device comprising:
2 a high resistivity polycrystalline layer;
3 a buried oxide layer over the polycrystalline
4 layer; and,
5 a silicon layer over the buried oxide layer.

1 4. The RF semiconductor device of claim 3
2 wherein the polycrystalline layer comprises a polysilicon
3 layer.

1 5. The RF semiconductor device of claim 3
2 further comprising an RF input.

1 6. The RF semiconductor device of claim 5
2 wherein the polycrystalline layer comprises a polysilicon
3 layer.

1 7. A method of fabricating an RF
2 semiconductor device comprising:
3 forming an oxide layer on a surface of a first
4 wafer, wherein the first wafer comprises low resistivity
5 silicon; and,
6 bonding the oxide layer of the first wafer to a
7 second wafer, wherein the second wafer comprises a high
8 resistivity polysilicon wafer, whereby the RF
9 semiconductor device is produced.

1 8. The method of claim 7 wherein the bonding
2 of the oxide layer of the first wafer to the second wafer
3 comprises:
4 implanting low atomic weight atoms in a surface
5 of the second wafer; and,
6 bonding the oxide layer of the first wafer to
7 the implanted surface of the second wafer.

1 9. The method of claim 7 wherein the bonding
2 of the oxide layer of the first wafer to the second wafer
3 comprises heating the first and second wafers so as to
4 bond the oxide layer of the first wafer to the second
5 wafer.

1 10. The method of claim 9 wherein the heating
2 of the first and second wafers so as to bond the oxide
3 layer of the first wafer to the second wafer comprises:
4 implanting low atomic weight atoms in a surface
5 of the second wafer; and,
6 heating the first and second wafers so as to
7 bond the oxide layer of the first wafer to the implanted
8 surface of the second wafer.

1 11. The method of claim 7 further comprising
2 processing the silicon of the first wafer to form an
3 integrated circuit of the RF semiconductor device
4 therein.

1 12. The method of claim 7 further comprising
2 processing the silicon of the first wafer to form
3 transistors and inductors.

1 13. A method of fabricating an RF
2 semiconductor device comprising:
3 forming a first oxide layer on a surface of a
4 first wafer, wherein the first wafer comprises a high
5 resistivity polycrystalline material;
6 forming a second oxide layer on a surface of a
7 second wafer, wherein the second wafer comprises low
8 resistivity silicon; and,
9 bonding the first and second oxide layers
10 against one another so as to produce the RF semiconductor
11 device.

1 14. The method of claim 13 wherein the
2 polycrystalline material comprises polysilicon.

1 15. The method of claim 13 further comprising
2 removing a portion of the silicon of the second wafer.

1 16. The method of claim 15 wherein the
2 removing of a portion of the silicon of the second wafer
3 comprises etching away the portion of the silicon of the
4 second wafer.

1 17. The method of claim 15 wherein the
2 removing of a portion of the silicon of the second wafer

3 comprises grinding away the portion of the silicon of the
4 second wafer.

1 18. The method of claim 15 wherein the
2 removing of a portion of the silicon of the second wafer
3 comprises etching and grinding away the portion of the
4 silicon of the second wafer.

1 19. The method of claim 13 wherein the bonding
2 of the first and second oxide layers against one another
3 comprises heating the first and second wafers so as to
4 bond the first and second oxide layers against one
5 another.

1 20. The method of claim 13 further comprising
2 processing the silicon of the second wafer to form an
3 integrated circuit of the RF semiconductor device
4 therein.

1 21. The method of claim 13 further comprising
2 processing the silicon of the second wafer to form
3 transistors and inductors.

1 22. A method of fabricating an RF
2 semiconductor device starting with a SOI wafer having a
3 top silicon layer, a buried oxide layer, and a bottom
4 silicon layer, the method comprising:
5 forming a new oxide layer on a surface of the
6 top silicon layer;
7 forming a high resistivity polysilicon layer
8 over the new oxide layer;
9 removing the bottom silicon layer of the SOI
10 wafer; and,
11 removing the buried oxide layer of the SOI
12 wafer so as to produce the RF semiconductor device.

1 23. The method of claim 22 wherein the forming
2 of a polysilicon layer over the new oxide layer comprises
3 depositing a polysilicon layer on the new oxide layer.

1 24. The method of claim 23 wherein the
2 removing of the bottom silicon layer of the SOI wafer
3 comprises grinding and/or etching away the bottom silicon
4 layer of the SOI wafer.

1 25. The method of claim 23 wherein the
2 removing of the buried oxide layer of the SOI wafer

3 comprises grinding and/or etching away the buried oxide
4 layer of the SOI wafer.

1 26. The method of claim 25 wherein the
2 removing of the bottom silicon layer of the SOI wafer
3 comprises grinding and/or etching away the bottom silicon
4 layer of the SOI wafer.

1 27. The method of claim 22 wherein the
2 removing of the bottom silicon layer of the SOI wafer
3 comprises grinding and/or etching away the bottom silicon
4 layer of the SOI wafer.

1 28. The method of claim 22 wherein the
2 removing of the buried oxide layer of the SOI wafer
3 comprises grinding and/or etching away the buried oxide
4 layer of the SOI wafer.

1 29. The method of claim 28 wherein the
2 removing of the bottom silicon layer of the SOI wafer
3 comprises grinding and/or etching away the bottom silicon
4 layer of the SOI wafer.

1 30. The method of claim 22 further comprising
2 processing the silicon remaining from the SOI wafer so as
3 to form an integrated circuit of the RF semiconductor
4 device therein.

1 31. The method of claim 22 further comprising
2 processing the silicon remaining from the SOI wafer so as
3 to form transistors and inductors.